



PATENT  
81788.0020

**AFTER FINAL RESPONSE UNDER 37 C.F.R. §1.116  
EXPEDITED PROCEDURE**

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

In re application of:

Shota Kitamura, et al.

Serial No: 09/392,865

Filed: September 9, 1999

For: **NON-VOLATILE SEMICONDUCTOR  
MEMORY DEVICE AND ITS  
MANUFACTURING METHOD**

Art Unit: 2811

Examiner: T. Tran

#15/ Amended  
R. Tyson  
1/23/01

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: BOX AF, Assistant Commissioner for Patents, Washington D.C. 20231, on	
January 5, 2001	Date of Deposit
William H. Wright	Name
<i>[Signature]</i>	Signature
1/5/01	Date

RECEIVED  
JAN 12 2001  
TECHNOLOGY CENTER  
2800

**AMENDMENT AND RESPONSE**

**UNDER 37 C.F.R. §1.116**

BOX AF  
Assistant Commissioner for Patents  
Washington, D.C. 20231

Dear Sir:

This is in response to the final Office Action dated July 5, 2000, which was paper #12 of the present application. Please amend the present application as follows:

**IN THE CLAIMS:**

*Sub D<sup>2</sup>*  
Please amend claim 17 as follows:

17. (Amended) The nonvolatile semiconductor memory device according to claim 16, [wherein] further comprising:

[memory regions extending in one direction and] element separating regions extending [in said] along one direction [are alternately formed;], wherein

*C1*  
[in each of said memory regions,] groups of said memory transistors are arranged [in] along said one direction and adjacent said element separating regions;

in each of said element separating regions, an element separating insulating film is formed on said substrate[, and extends] extending in said one direction;